ChainMap: Depth-Optimal Mapping of Logic Chains in Reconfigurable Fabrics

APPLICATION AREAS
FPGA (Field Programmable Gate Array) Computer Aided Design, VLSI (Very Large Scale Integration) Computer Aided Design

ABSTRACT
Look-up table (LUT)-based FPGA have typically been used in prototyping rather than as critical design elements. However, performance improvements have advanced FPGAs to being valuable in development of end-components. An important dedicated structure found in currently available architectures is the arithmetic carry chain. However, in designs that incorporate limited arithmetic operations and contain a carry-select style architecture, the carry chain is an under utilized resource. To overcome this deficiency, ISU researchers have developed a novel algorithm, ChainMap, for depth-optimal mapping of logic chains in reconfigurable fabrics. ChainMap establishes a difference between programmable routing connections and chain connections, and optimally identifies them without requiring the use of a user-specified hardware description language (HDL). In addition, ChainMap allows the use of non-arithmetic as well as arithmetic chains. As a result, significant performance gains are achievable for all designs and design flow is freer.

BENEFITS
ChainMap is:
- Effective (experimental results indicate that ChainMap improves performance up to 40% compared to HDL methods)
- Efficient (allows the use of non-arithmetic operations and does not require the preservation of HDL macros through the design flow)
- Flexible (eliminates the need for HDL to create logic chains and frees the design flow)

RELATED TECHNOLOGIES
This technology is related to ISURF #3630, Logic Element Architecture for Generic Logic Chains in Programmable Devices

REFERENCES
Conference proceedings: “Beyond the arithmetic constraint: depth-optimal mapping of logic chains in LUT-based FPGAs”, Michael T. Frederick and Arun Somani, FPGA ’08, February 24-26, Monterrey, CA.


INVENTOR(S)
Drs. Michael T. Frederick and Arun K. Somani (Electrical and Computer Engineering)

INTELLECTUAL PROPERTY STATUS (February 2014)
Patents issued: US Patent Nos. 8,438,522 and 8,661,394

LICENSING CONTACT
Jay Bjerke  
E-mail: licensing@iastate.edu  
Phone: 515-294-3621 (Direct Line)